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BEVER HOFFMAN & HARMS, LLP 1432 CONCANNON BLVD BLDG G LIVERMORE, CA 94550-6006			PROCTOR, JASON SCOTT	
			ART UNIT	PAPER NUMBER
			2123	

DATE MAILED: 07/19/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/025,414	TSAI ET AL.	
	Examiner	Art Unit	
	Jason Proctor	2123	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 27 April 2005.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-20 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-20 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|---|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

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DETAILED ACTION

Claims 1-20 were presented for examination and rejected in Office Action dated March 1, 2005.

Claims 1, 4-5, 7-11, 14, 17, and 20 have been amended in Applicants' response dated April 27, 2005. Claims 1-20 remain pending in this application.

Claims 1-20 have been rejected.

Response to Rejections under 35 U.S.C. § 112

Regarding the rejections of claims 1-6 and 17-20 under 35 U.S.C. § 112, first paragraph, as failing to comply with the enablement requirement, the Examiner thanks Applicants for providing clarifying remarks. The Examiner appreciates the clarification that the invention relates to a database, as stated on page 8:

Therefore, the simulation itself is not the object of Applicants' invention. Rather, the invention relates to a novel database that can capture information regarding that simulation to minimize the need to repeat the simulation process.

The Examiner appreciates Applicants' example of typical use of the database, as stated on page 8:

In contrast, the actual deviation (e.g. +12 nm) of a control point can be captured in Applicants' recited database. In this case, if the user changes the tolerance from 10 nm, the database can easily be searched to find any deviations greater than 10 nm (e.g. 11 nm, 12 nm, 13 nm, etc.).

These and related clarifying remarks show that the database stores the data output from the single simulation process. By specifying a particular tolerance, the database can provide those control points that exhibit deviations beyond the specified tolerance.

The method of simulation required to enable Applicants' invention formed the basis for the previous rejection. Applicants' remarks have clarified that the simulation method could be

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according to prior art methods and does not require an inventive simulation. Applicants' arguments have been fully considered and have been found persuasive. The previous rejection of claims 1-6 and 17-20 under 35 U.S.C. § 112, first paragraph, have been withdrawn.

Regarding the rejections of claims 6 and 16 under 35 U.S.C. § 112, first paragraph, as failing to comply with the enablement requirement, the Examiner thanks Applicants for providing clarifying remarks. Applicants have fulfilled the Examiner's request to cite support in the disclosure for the limitations of claims 6 and 16. It is clear from the paragraphs cited that the "one new rule associated with the plurality of control points" refers to a rule defining a group of control points and does not require repeating the step of simulation, as exemplified in paragraph 0025:

Each type of control point can be further characterized by assigning it a rule identification. For example, edge type control points can be divided into groups by a feature width w [...].

Applicants' arguments have been fully considered and have been found persuasive. The previous rejection of claims 6 and 16 under 35 U.S.C. § 112, first paragraph, has been withdrawn.

Regarding the rejection of claims 7-16 under 35 U.S.C. § 112, first paragraph, as claiming a scope of invention not commensurate with the scope of the disclosure, the Examiner thanks Applicant for amending the language of these claims. Claims 7-16, as amended, are commensurate in scope with the disclosure. The previous rejection of claims 7-16 under 35 U.S.C. § 112, first paragraph, has been withdrawn.

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Regarding the rejection of claims 4, 5, 7, 14, 15, 17, and 20 under 35 U.S.C. § 112, second paragraph, the Examiner thanks Applicant for amending the claim language to address the issues raised in the previous Office Action. However, these amendments appear to have inadvertently omitted the replacement of the phrase "the certain" with "the subset of" in claim 20, as was amended in claim 4. The rejections of claims 4, 5, 7, 14, and 15 have been withdrawn. The rejection of claim 20 regarding the phrase "the certain information" is maintained, however the Examiner has interpreted this claim in anticipation that it will be amended in accordance with claim 4.

Response to Rejections under 35 U.S.C. § 103

Regarding the rejection of claims 1-20 under 35 U.S.C. § 103(a) as being unpatentable over US Patent No. 6,757,645 to Chang et al. (Chang) in view of US Patent No. 6,263,301 to Cox, the Examiner has withdrawn these rejections in light of the amendments to the claims. Applicants' arguments regarding these references are therefore moot, however the Examiner will address several points in the interest of expediting prosecution.

Applicants' arguments refer to a description of the disclosed invention in paragraph 0008 of the specification:

Advantageously, based on the database, a user can easily change information regarding the rule identification, tolerance, and target parameter and still generate valid reports. Because a simulation a layout need only be done once and accessing a database is significantly faster than simulating a layout, these reports can be expeditiously generated.

This and other portions of the disclosure describe a system wherein simulation data is repeatedly queried to produce reports of e.g. design rule check (DRC) violations where, in the prior art, each query requires a new simulation to be performed. This results in a particular type of report that

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is directly related to the e.g. design rule check. However, the claimed invention (exemplified in claim 1) broadly recites:

extracting a subset of information from the database to generate the reports using a first set of checking parameters, wherein extracting is repeatable with a second set of checking parameters without repeating the steps of providing, performing, and storing.

This particular limitation would be taught by almost any conventional, repeatable database query. Regardless of how the data is inserted into a conventional database, it is generally well known to query the database with different parameters without requiring that the data be regenerated and reinserted into the database. The “checking parameters” are not positively recited as related to a design rule check. Therefore Applicants’ arguments directed to the disclosed invention are not fully represented by the claim limitations and therefore would be unpersuasive. As noted above, the previous rejections under 35 U.S.C. § 103 have been withdrawn in light of the amendments to the claims.

Further, regarding the teachings related to the meaning of “control points,” the specification at paragraph 0022 broadly teaches that:

After dissection, each segment can be designated using an associated control point (sometimes located at the mid-point of the segment). By using a control point, a tool can efficiently operate on its associated segment. Specifically, operations performed on a control point affect its associated segment in a similar manner. For example, if the control point is biased in an optical proximity correction (OPC) operation by a distance X, then its associated segment is also biased by distance X.

Although Applicants’ invention may employ a particular definition of a “control point,” this exemplary teaching does not appreciably distinguish a “control point” from a point defining a polygon, as is conventionally used in the prior art to represent a circuit layout. For example, where a layout is defined in part with a rectangle with corners defined as “control points,” operations (such as moving the corners) would affect the associated segments in a similar

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manner by reshaping the rectangle to correspond to the new corner point locations. This is particularly relevant because it is known in the art to represent an IC layout using a number of polygons and to manipulate those polygons in order to correct DRC violations.

Outstanding Rejections

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claim 20 is rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 20 recites "creating a temporary table for the certain information" but offers no explanation of what constitutes "certain information". The recitation of "the certain information" lacks antecedent basis as the result of what appears to be an inadvertently omitted amendment to the claim language. The Examiner presumes the limitations of claim 20 should be interpreted according to the limitations of claim 4.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

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(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1-20 are rejected under 35 U.S.C. 102(b) as being anticipated by "Lavenir CAM Software User's Guide" by Lavenir, copyright 1999.

Regarding claim 1, Lavenir discloses a method of generating reports regarding an integrated circuit layout [*"Vector DRC uses the Gerber description of the position, size, and shape of elements to determine clearance and contact between elements."* (page 385); *"Text Error Report"* (page 404)], the method comprising:

Providing a plurality of control points associated with the integrated circuit layout [pads, traces, etc. shown in simulated IC layout on page 407; *"You can insert all types of data: pads and traces; special classes of traces and trace combinations such as orthogonals, 90-degree pairs, rectangular polygons, elbows; several types of arcs such as circles, 3-points arcs, chord and tangent arcs, chord and point arcs, center and chord arcs; and text."* (page 115)];

Performing a single simulation of the plurality of control points [*"The best Vector Design Rule Check results are obtained from plot data that has been prepared."* (page 399) Prepared plot data constitutes a "simulation" as a model of an IC layout. See, for example, page 407, showing a portion of a computer simulation of an IC layout; *"Vector DRC uses the Gerber description of the position, size, and shape of elements to determine clearance and contact between elements."* (page 385)];

Storing information from the single simulation in a database [*"The process [Vector Design Rule Check] examines individual layers [...] or the entire database, depending on how you set it up."* (page 399) The simulated IC layout is clearly stored in a database.]

wherein the information includes deviation information for at least one control point, the deviation information indicating a deviation of a simulated location from a corresponding location on the integrated circuit layout [“*gap settings*” constitutes a deviation, as in “*The system flags elements that are closer together than the minimum acceptable air gap,*” (page 402); “*The system flags elements*” constitutes “deviation information” (page 402); and features such as “*Trace*”, “*Pad*”, and “*Soldermask*”, etc. constitute “control points.” (page 402) These gap settings are clearly in reference to the simulated location of circuit elements in the simulated IC layout shown on page 407]; and

Extracting a subset of information from the database to generate the reports [“*Maximum errors,*” “*The system gives you the option to abort a DRC when it hits this number*” (page 405); alternatively, “*Reference Frame,*” “*If you want to check only a portion of the plot*” (page 404)] using a first set of checking parameters [“*gap settings*” in the “*Rules*” tab (page 402)], wherein extracting is repeatable with a second set of checking parameters without repeating the steps of providing, performing, and storing [“*Remove Vector Design Rule Check Errors Flags from the Plot*” (page 408) and subsequently “*Run the Vector Design Rule Check*” (page 401) on the previously “prepared plot data” (page 399)].

Regarding claim 2, Lavenir discloses that providing a plurality of control points comprises designating a tolerance [“*Air Gap Violations: The system flags elements that are closer together than the minimum acceptable air gap.*” (page 402)].

Regarding claim 3, Lavenir discloses that storing information includes organizing the information in at least a statistics table [*"The program can generate a Distance Histogram report to verify the manufacturability of plot data and aid in the quoting process. The Distance Histogram report is a text file that includes the number of times each particular clearance occurs in the plot."* (page 409)].

Regarding claim 4, Lavenir discloses creating a temporary table for the subset of information wherein the temporary table is separate from the database [*"The program can generate a Distance Histogram report to verify the manufacturability of plot data and aid in the quoting process. The Distance Histogram report is a text file that includes the number of times each particular clearance occurs in the plot."* (page 409)].

Regarding claim 5, Lavenir discloses viewing the subset of information in at least a histogram mode [*"The program can generate a Distance Histogram report to verify the manufacturability of plot data and aid in the quoting process. The Distance Histogram report is a text file that includes the number of times each particular clearance occurs in the plot."* (page 409)].

Regarding claim 6, Lavenir discloses providing a rule associated with the plurality of control points [*"Violations D Code" "Each type of error is automatically mapped to a different D Code for easy identification"* (page 405); *"To see all instances of a particular type of violation, query the properties of a selected error flag, set the selection criteria to look for only*

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that D Code, and use the First Element and Next Element commands.” (page 407)] and storing new information in the database based on the at least one new rule and the single simulation [“View Vector Design Rule Check Errors On Screen” “Violations are flagged by inserting selected elements of the Violation D Codes on the original layers” (page 407); in conjunction with “The process examines individual layers [...] or the entire database, depending on how you set it up.” (page 399); the Vector Design Rule Check flags violations by adding information to the database storing the simulated IC layout].

Regarding claim 7, Lavenir discloses a database for reporting results from simulating an integrated circuit layout [“The process examines individual layers [...] or the entire database, depending on how you set it up.” (page 399); The simulated IC layout is clearly stored in a database. “The best Vector Design Rule Check results are obtained from plot data that has been prepared.” (page 399) Prepared plot data constitutes a “simulation” as a model of an IC layout. See, for example, page 407, showing a portion of a computer simulation of an IC layout] the database comprising:

A plurality of control points associated with the integrated circuit layout and information regarding the plurality of control points [pads, traces, etc. shown in simulated IC layout on page 407; “You can insert all types of data: pads and traces; special classes of traces and trace combinations such as orthogonals, 90-degree pairs, rectangular polygons, elbows; several types of arcs such as circles, 3-points arcs, chord and tangent arcs, chord and point arcs, center and chord arcs; and text.” (page 115)]; and

Deviation information regarding the plurality of control points, wherein the deviation information indicates deviations of simulated locations from corresponding locations on the integrated circuit layout [“*gap settings*” constitutes a deviation, as in “*The system flags elements that are closer together than the minimum acceptable air gap,*” (page 402); “*The system flags elements*” constitutes “deviation information” (page 402); and features such as “*Trace*”, “*Pad*”, and “*Soldermask*”, etc. constitute “control points.” (page 402) These gap settings are clearly in reference to the simulated location of circuit elements in the simulated IC layout shown on page 407], the deviation information including a magnitude of each deviation [“*gap settings*” (page 402) are a measure of magnitude; flagged elements represent a deviation with a magnitude that exceeds the “minimum acceptable air gap”].

Regarding claim 8, Lavenir discloses including a spacing for each control point related to an edge of the simulated IC layout [“*Outline to copper area*” (page 402); “*The system flags any copper area elements that are closer than the minimum distance to the board outline.*” (page 403)].

Regarding claim 9, Lavenir discloses that the information includes at least a type for each control point “*You can insert all types of data: pads and traces; special classes of traces and trace combinations such as orthogonals, 90-degree pairs, rectangular polygons, elbows; several types of arcs such as circles, 3-points arcs, chord and tangent arcs, chord and point arcs, center and chord arcs; and text.*” (page 115)].

Regarding claim 10, Lavenir discloses that storing information includes organizing the information in at least a statistics table [*"The program can generate a Distance Histogram report to verify the manufacturability of plot data and aid in the quoting process. The Distance Histogram report is a text file that includes the number of times each particular clearance occurs in the plot."* (page 409)].

Regarding claim 11, Lavenir discloses a method of generating simulation reports regarding an integrated circuit layout [*"Vector DRC uses the Gerber description of the position, size, and shape of elements to determine clearance and contact between elements."* (page 385); *"Text Error Report"* (page 404)], the method comprising:

Dissecting feature edges on the integrated circuit layout into segments, each segment including a control point [*"Vector DRC uses the Gerber description of the position, size, and shape of elements to determine clearance and contact between elements."* (page 385)];

Performing a single simulation of the plurality of control points [*"The best Vector Design Rule Check results are obtained from plot data that has been prepared."* (page 399) Prepared plot data constitutes a "simulation" as a model of an IC layout. See, for example, page 407, showing a portion of a computer simulation of an IC layout; *"Vector DRC uses the Gerber description of the position, size, and shape of elements to determine clearance and contact between elements."* (page 385)];

Storing information from the single simulation in a database [*“The process [Vector Design Rule Check] examines individual layers [...] or the entire database, depending on how you set it up.”* (page 399) The simulated IC layout is clearly stored in a database.]

wherein the information includes deviation information for at least one control point, the deviation information indicating a deviation of a simulated location from a corresponding location on the integrated circuit layout [*“gap settings”* constitutes a deviation, as in *“The system flags elements that are closer together than the minimum acceptable air gap,”* (page 402); *“The system flags elements”* constitutes “deviation information” (page 402); and features such as *“Trace”*, *“Pad”*, and *“Soldermask”*, etc. constitute “control points.” (page 402) These gap settings are clearly in reference to the simulated location of circuit elements in the simulated IC layout shown on page 407]; and

Extracting user-identified information from the database to generate the reports [*“select the type of Design Rule Violations to include in the Vector Design Rule Check”* (page 402); *“If you want to output a text error report, click the Output a Text Error Report option”* (page 404)].

Regarding claim 12, Lavenir discloses that the information includes at least a type for each control point *“You can insert all types of data: pads and traces; special classes of traces and trace combinations such as orthogonals, 90-degree pairs, rectangular polygons, elbows; several types of arcs such as circles, 3-points arcs, chord and tangent arcs, chord and point arcs, center and chord arcs; and text.”* (page 115)].

Regarding claim 13, Lavenir discloses that storing information includes organizing the information in at least a statistics table [*"The program can generate a Distance Histogram report to verify the manufacturability of plot data and aid in the quoting process. The Distance Histogram report is a text file that includes the number of times each particular clearance occurs in the plot."* (page 409)].

Regarding claim 14, Lavenir discloses creating a temporary table for user-specified information wherein the temporary table is separate from the database [*"The program can generate a Distance Histogram report to verify the manufacturability of plot data and aid in the quoting process. The Distance Histogram report is a text file that includes the number of times each particular clearance occurs in the plot."* (page 409)].

Regarding claim 15, Lavenir discloses viewing the subset of information in at least a histogram mode [*"The program can generate a Distance Histogram report to verify the manufacturability of plot data and aid in the quoting process. The Distance Histogram report is a text file that includes the number of times each particular clearance occurs in the plot."* (page 409)].

Regarding claim 16, Lavenir discloses providing a rule associated with the plurality of control points [*"Violations D Code"* *"Each type of error is automatically mapped to a different D Code for easy identification"* (page 405); *"To see all instances of a particular type of violation, query the properties of a selected error flag, set the selection criteria to look for only*

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that D Code, and use the First Element and Next Element commands.” (page 407)] and storing new information in the database based on the at least one new rule and the single simulation [“View Vector Design Rule Check Errors On Screen” “Violations are flagged by inserting selected elements of the Violation D Codes on the original layers” (page 407); in conjunction with “The process examines individual layers [...] or the entire database, depending on how you set it up.” (page 399); the Vector Design Rule Check flags violations by adding information to the database storing the simulated IC layout].

Claims 17-20 recite an apparatus with means for performing the method of claims 1-4. As Lavenir teaches a computer program (Lavenir reference is a “*Lavenir CAM Software User’s Guide*” (copyright page)] that would be executed by a computer system, thus forming an apparatus that performs the methods of the computer program, claims 17-20 are rejected for the same reasons given above for claims 1-4.

Conclusion

Art considered pertinent by the examiner but not applied has been cited on form PTO-892.

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

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A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jason Proctor whose telephone number is (571) 272-3713. The examiner can normally be reached on 8:30 am-4:30 pm M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Leo Picard can be reached at (571) 272-3749. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.

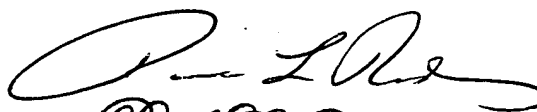
Any inquiry of a general nature or relating to the status of this application should be directed to the TC 2100 Group receptionist: 571-272-2100. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>.

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Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Jason Proctor
Examiner
Art Unit 2123

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Paul L. Rodriguez 7/14/05
Primary Examiner
Art Unit 2125